

CERTIFICATE OF TRANSMISSION BY FACSIMILE (37 CFR 1.8)

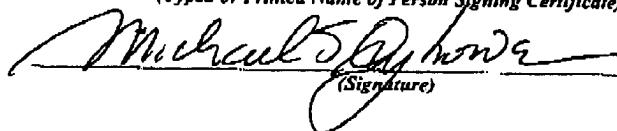
Applicant(s): Hiroshi KIMURA

Docket No.

121056-020

Serial No.
09/837,022Filing Date
April 18, 2001Examiner
James MitchellGroup Art Unit
2827

Invention:

SEMICONDUCTOR DEVICE, ITS MANUFACTURING METHOD AND ELECTRO DEPOSITION FRAMEI hereby certify that this Declaration Under 37 CFR 1.132 by Mr. Hiroshi KIMURA
*(Identify type of correspondence)*is being facsimile transmitted to the United States Patent and Trademark Office (Fax. No. 703-872-9306)on February 9, 2004
*(Date)*Michael S. Gzybowski*(Typed or Printed Name of Person Signing Certificate)*
*(Signature)*RECEIVED
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PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Group
Art Unit: 2827

Attorney
Docket No.: 121056-020

Applicant: Hiroshi KIMURA

Invention: SEMICONDUCTOR DEVICE, ITS
MANUFACTURING METHOD
ELECTRO DEPOSITION FRAME AND

Serial No.: 09/837,022

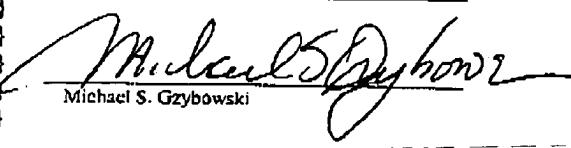
Filed: April 18, 2001

Examiner: James Mitchell

Certificate Under 37 CFR 1.8(f)

I hereby certify that this correspondence is being transmitted to the United States Patent and Trademark Office via facsimile transmission on the date indicated below.

on February 9, 2004



Michael S. Gzybowski

TRANSMITTAL OF KIMURA DECLARATION UNDER 37 CFR §1.132

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Further to appellants' Brief on Appeal filed January 30, 2004, appellants are submitting a signed copy of Mr. Hiroshi KIMURA's Declaration under 37 C.F.R. §1.132.

Respectfully submitted,



Michael S. Gzybowski
Reg. No. 32,816

BUTZEL LONG
350 South Main Street
Suite 300
Ann Arbor, Michigan 48104
(734) 995-3110

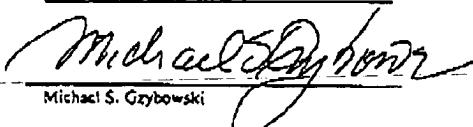
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2004年 2月 9日 16時47分

734 995 1777 TO 917038729306 P.03/05
NO. 2107 P. 2

Appl. No. 09/837,022

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

<i>Group</i>	2827	}	RESPONSE AFTER FINAL REJECTION
<i>Art Unit:</i>			EXPEDITED PROCESSING REQUESTED
<i>Attorney</i>	121056-020	}	<u>Certificate Under 37 CFR 1.8(b)</u>
<i>Docket No.:</i>			I hereby certify that this correspondence is being transmitted to the United States Patent and Trademark Office via facsimile transmission on the date indicated below.
<i>Applicant:</i>	Hiroshi KIMURA	}	on <u>December 15, 2003</u> MSG
<i>Invention:</i>			SEMICONDUCTOR DEVICE, ITS MANUFACTURING METHOD AND ELECTRO DEPOSITION FRAME
<i>Serial No.:</i>	09/837,022	}	
<i>Filed:</i>			April 18, 2001
<i>Examiner:</i>	James Mitchell		Michael S. Ozybowski

DECLARATION BY MR. HIROSHI KIMURA SUBMITTED UNDER 37 CFR §1.132

Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

I, Hiroshi KIMURA, hereby declare and say as follows:

1. I am currently employed as the director of the Management Division Package Technical Department of Torex Semiconductor Ltd. In my present position I am responsible for unifying the development, design and mass production of semiconductor packages for my company's manufacturing line.

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2. That my educational background includes four (4) years of studying Material Engineering in the Applied Chemical course in the Engineering Department of Toyo University.
3. That after completing my study at the Engineering Department of Toyo University I became employed by Torex Semiconductor Ltd. where I have researched electric/electronic materials and have been engaged with the production of resin-packaged products for twenty (20) years.
4. That I am the inventor of U.S. Patent Application Serial No. 09/837,022 and am familiar with the pending specification and claims.
5. That I am familiar with the Office Action mailed July 1, 2003 in U.S. Patent Application Serial No. 09/837,022.
6. That I am familiar with the prior art references cited and relied upon by Examiner James Mitchell in Office Action mailed July 1, 2003 in U.S. Patent Application Serial No. 09/837,022 and particularly with U.S. Patent Application Publication No. 2002/0100165 to Glenn.
7. That electroforming techniques (Electro-Casting or Electrodeposition) have been generally applied to ornaments, but have not been applied to the field of electronic products, so that such techniques are not familiar to those in the field of electronic products.
8. That in the invention set forth and claimed in U.S. Patent Application Serial No. 09/837,022 the application of electrodeposition does not produce an alloy between the metallic substrate and the metallic layer 8. Accordingly, the metal substrate 9 can be easily removed from the resin sealing body 11.

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9. That, since removal of the metal substrate 9 from the resin sealing body 11 before the steps of wiring and resin sealing cannot lead to the production of semiconductor devices, the contact strength between the metallic substrate and the metallic layer must be maintained.

10. That in the case of metallic substrates, the contact strength can be adjusted by suitably etching the surface of the metallic substrate before electrodeposition of the metallic layer.

11. That using electrodeposition for making a lead frame and using related techniques such as etching to provide a suitable contact strength between a metallic substrate and a metallic layer are techniques that belong to a different technical field than the techniques of applying a metal layer to a plastic substrate.

12. That therefore, it follows that one of ordinary skill in the art reading Glenn would avoid using a metal substrate and would not consider of replacing the plastic substrate of Glenn with a metal substrate.

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

JANUARY 30, 2004

Date

1051921

HIROSHI KIMURA

Signature